Modern flash devices require only a single supply voltage and contain on-chip circuitry to create the nonstandard programming and erasure voltages required by the memory array. Control logic determines which block is placed into erase or program mode at any given time as requested by the microprocessor with a predefined flash control algorithm. AMD's algorithm consists of six special write transactions to the flash: two unlock cycles, a setup command, two more unlock cycles, and the specific erase command. This sequence is detailed in Table 4.1. If interrupted, the sequence must be restarted to ensure integrity of the command.

TABLE 4.1 29LV010B/29LV001B Erase Sequence*

Cycle	Write Address	Write Data
1	0x555	0xAA
2	0x2AA	0x55
3	0x555	0x80
4	0x555	0xAA
5	0x2AA	0x55
6	Erase address	Erase command

**Source:* Am29LV001B, Pub#21557, and Am29LV010B, Pub #22140, Advanced Micro Devices, 2000.

For a whole-chip erase, the address/data in cycle 6 is 0x555/0x10. For a single-sector erase, the address/data in cycle 6 is the sector address/0x30. Multiple erase commands may be queued together to reduce the total time spent by the internal control logic erasing its sectors. While executing commands, the data bus is converted into a status communication mechanism. The microprocessor is able to periodically poll the device by reading from any valid address. While the erase is in progress, a value other than 0xFF will be returned. As soon as the erase has completed, the microprocessor will read back 0xFF.

Writes to previously erased flash memory locations are accomplished with a similar technique. For each location to be programmed, a four-cycle program command sequence is performed as shown in Table 4.2. Again, the microprocessor polls for command completion by reading from the device. This time, however, the address polled must be the write address. When the microprocessor reads back the data that it has written, the command is known to have completed.

TABLE 4.2 29LV010B/29LV001B Programming Sequence

Cycle	Write Address	Write Data
1	0x555	0xAA
2	0x2AA	0x55
3	0x555	0xA0
4	Write address	Write data

Other ancillary commands are supported, including device reset and identification operations. The 29LV001B includes a hardware-reset signal in addition to the soft reset command. Identification

enables the microprocessor to verify exactly which flash device it is connected to and which sectors have been hardware protected. Identification is useful for a removable flash module that can be built with different parts for specific capacities. Protection status is useful so that software running on the microprocessor can know if it is possible to program certain areas of the memory.

Hardware sector protection is accomplished during the time of system manufacture by applying a higher than normal voltage to designated pins on the flash device using special equipment. The designated pins on the 29LV010B/29LV001B are address bit 9, A9, and the output enable, OE*. These pins are driven to 12 V while the address of the sector to be protected is applied to other address pins. During normal operation, there is no way for 12 V to be driven onto these signals, preventing the protected sectors from being unprotected while in circuit. The exception to this is a feature on the 29LV001B that AMD calls *temporary sector unprotect*. Previously protected sectors can be temporarily unprotected by driving 12 V onto the RESET* pin with specific circuitry for this purpose. Taking advantage of this feature makes it possible to modify the most sensitive areas of the flash by locating a hardware unprotect enable signal in a logic circuit separate from the flash chip itself.

The major difference between the 29LV010B and 29LV001B is their sector organization. The 29LV010B contains 8 uniform sectors of 16 kB each. The 29LV001B contains 10 sectors of nonuniform size. Two variants of the 29LV010B are manufactured by AMD, top and bottom boot sector architectures, and their sector organization is listed in Table 4.3.

TABLE 4.3 29LV010B Sector Organization

Sector Number	Top Boot Sector	Bottom Boot Sector
0	16 kB	8 kB
1	16 kB	4 kB
2	16 kB	4 kB
3	16 kB	16 kB
4	16 kB	16 kB
5	16 kB	16 kB
6	16 kB	16 kB
7	4 kB	16 kB
8	4 kB	16 kB
9	8 kB	16 kB

The reason for these mirrored architectures is that some microprocessors contain reset vectors toward the top of their address space and some toward the bottom. It is a better fit to locate the boot sectors appropriately depending on a system's CPU. As with any complex IC, there are many details relating to the operation of these flash ICs. Refer to AMD's data sheets for more information.

4.4 EEPROM

Electrically erasable programmable ROM, or EEPROM, is flash's predecessor. In fact, some people still refer to flash as "flash EEPROM," because the underlying structures are very similar. EEPROM,